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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,646	03/16/2001	Shunpei Yamazaki	12732-021001 / US4802	5011

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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/809,646	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Thoi V Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-35* is/are pending in the application.

4a) Of the above claim(s) *10,12,14,16-21,23-25,29 and 31-35* is/are withdrawn from consideration.

5)☒ Claim(s) *11,13,15 and 30* is/are allowed.

6)☒ Claim(s) *1-9 and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0504*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 14, 2004 has been entered.

Accordingly, claims 1-3 were amended, claim 22 was cancelled, and claims 10, 12, 14, 16-21, 23-25, 29, and 31-35 were withdrawn. Currently, claims 1-9, 11, 13, 15, 26-28 and 30 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 2, 4 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Ha (USPN 5,767,530).

Re claim 1, as shown in Figs. 4A-4G, Ha discloses a liquid crystal display device comprising:

a semiconductor layer 32 formed on an insulating surface 31, said semiconductor layer having a channel forming region 32d, an LDD region 32a and source and drain regions 32b, 32c;

a gate insulating film 33 formed on said semiconductor layer;

a first gate electrode 36a, 34, 36b formed on said gate insulating film (col. 4, lines 51-55);

a second gate electrode 35 formed on said first gate electrode,

wherein the width of said first gate electrode in the longitudinal direction of said channel forming region is larger than that of said second gate electrode (Fig. 4G);

wherein said LDD region 32a entirely overlaps with said first gate electrode 36a, 34, 36b with said gate insulating film 33 interposed therebetween and contacts said source and drain regions 32b, 32c (Fig. 4G).

Re claim 2, said channel forming region 32d overlaps with said second gate electrode with said gate insulating film 33 interposed therebetween.

Re claims 4 and 5, Ha discloses that the LDD region is formed in a self-aligning manner in accordance with the addition of an impurity element into said semiconductor laver with said second gate electrode as a mask (see Abstract).

5. Claims 1, 2, 4, 5, 7, 8, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (USPN 6,369,410 B1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Re claim 1, as shown in Figs. 1A and 1B, Yamazaki et al. discloses a liquid crystal display device comprising:

a semiconductor layer formed on an insulating surface 102, said semiconductor layer having a channel forming region 107, an LDD region 108 and source and drain regions 109;

a gate insulating film 104 formed on said semiconductor layer;

a first gate electrode 110, 112 formed on said gate insulating film;

a second gate electrode 105, 111 formed on said first gate electrode,

wherein the width of said first gate electrode 110, 112 in the longitudinal direction of said channel forming region is larger than that of said second gate electrode 105, 111;

wherein said LDD region 108 entirely overlaps with said first gate electrode 110, 112 with said gate insulating film 104 interposed therebetween (Fig. 5) and contacts said source and drain regions 109.

Re claim 2, said channel forming region 107 overlaps with said second gate electrode 105, 111 with said gate insulating film 104 interposed therebetween.

Re claims 4 and 5, Yamazaki discloses that the LDD region is formed in a self-aligning manner in accordance with the addition of an impurity element into said semiconductor laver with said second gate electrode as a mask (col. 15, lines 27-36),

wherein, re claims 7 and 8, said LDD region contains a region having a concentration of said impurity element gradient in a range from at least 1x10 to 1x10 atoms/cm3, while increasing as the distance from said channel forming region increasing (col. 21, lines 4-11).

Finally, with respect to claims 26 and 27, as intended use, the liquid crystal display device of Yamazaki is incorporated into an electronic equipment selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game apparatus, a car navigation system, a personal computer and a portable information terminal as shown in Figs. 29A to 29F (col. 51, lines 30-36).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 6 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (USPN 6,462,802 B1) in view of Ha (USPN 5,767,530).

Re claim 3, as shown in Fig. 1, Nishimura et al. discloses a liquid crystal display device comprising:

a semiconductor layer formed on an insulating surface 104, said semiconductor layer having a channel forming region 105, and source and drain regions 109;

a gate insulating film 106 formed on said semiconductor layer;

a first gate electrode 107 formed on said gate insulating film, said first gate electrode having a tapered shape in cross section at an edge portion; and

a second gate electrode 108 formed on said first gate electrode,

wherein the width of said first gate electrode 107 in the longitudinal direction of said channel forming region is larger than that of said second gate electrode 108;

Nishimura et al. discloses a liquid crystal display that is basically the same as that recited in claim 3 except for an LDD region.

As shown in Fig. 4G, Ha discloses a liquid crystal display comprising an LDD region 32a formed in a semiconductor layer for reducing leakage current (col. 3, lines 10-17 and col. 7, lines 39-43),

wherein said LDD region 32a entirely overlaps with a first gate electrode 36a, 34, 36b with a gate insulating film 33 interposed therebetween and contacts source and drain regions 32b, 32c; and

wherein a channel forming region 32d overlaps with a second gate electrode 35 with said gate insulating film 33 interposed therebetween.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the liquid crystal display device of Nishimura et al. with the teaching of Ha by forming an LDD region for reducing leakage current (col. 7, lines 39-43).

Re claim 6, Ha discloses that the LDD region is formed in a self-aligning manner in accordance with the addition of an impurity element into said semiconductor laver with said second gate electrode as a mask (see Abstract).

Re claim 28, it is obvious that, for intended use, the liquid crystal display device is incorporated into an electronic equipment such as a camera, a projector, a personal computer and/or a portable information terminal.

8. Claims 7, 8, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ha (USPN 5,767,530) in view of JP 6-148685 (JP'685).

The liquid crystal display device of Ha includes all that is recited in claims 7 and 8 except for said LDD region containing a region having a concentration of said impurity

element gradient in a range from at least 1x10^{17} to 1x10^{18} atoms/cm3 , while increasing as the distance from said channel forming region increasing.

JP'685 discloses an LDD structure manufactured by ion implantation wherein a concentration of impurity element gradient is 1x10^{17} atoms/cm3 , while increasing as the distance from a channel forming region (below the gate structure) increasing so as to minimize a drain leakage current (paragraphs 20 and 25)

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the liquid crystal display device of Ha with the teaching of Kim et al. by forming an LDD region containing a region having a concentration of said impurity element gradient of at least 1x10 atoms/cm3 for minimizing the drain leakage current (paragraph 25).

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (USPN 6,462,802 B1) in view of Ha (USPN 5,767,530) as applied to claims 3, 6 and 28 above and further in view of JP 6-148685 (JP'685).

The liquid crystal display device of Nishimura et al. in view of Ha above includes all that is recited in claim 9 except for said LDD region containing a region having a concentration of said impurity element gradient in a range from at least 1x10^{17} to 1x10^{18} atoms/cm3, while increasing as the distance from said channel forming region increasing.

JP'685 discloses an LDD structure manufactured by ion implantation wherein a concentration of impurity element gradient is 1x10^{17} atoms/cm3 , while increasing as the

distance from a channel forming region (below the gate structure) increasing so as to minimize a drain leakage current (paragraphs 20 and 25)

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the liquid crystal display device of Nishimura et al. with the teaching of JP'685 by forming an LDD region containing a region having a concentration of said impurity element gradient of at least 1x10 atoms/cm3 for minimizing the drain leakage current (paragraph 25).

Allowable Subject Matter

10. Claims 11, 13, 15 and 30 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claim 11, none of the prior art of record discloses, in combination with other limitations as claimed, a liquid crystal display device comprising a pixel TFT and a driver circuit TFT, wherein the semiconductor layer of said driver circuit TFT comprises:

a third LDD region contacting the channel forming region and entirely overlapping with the first gate electrode with said gate insulating film interposed therebetween; and

a source region and a drain region contacting said third LDD region,

wherein the first gate electrode has a tapered shape in cross section at an edge portion; and

wherein the width of the first gate electrode in the longitudinal direction of the channel forming region is larger than that of the second gate electrode formed on the first gate electrode.

The most relevant references, USPN 6,365,917 B1 of Yamakazi (US'917) and USPN 6,369,410 B1 of Yamazaki et al. (US'410), disclose the formation of the third LDD region. However, these references are overcome by a statement of common ownership submitted by Applicant on June 14, 2004.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

12/03/2004

TARIFUR R. CHOWDHURY
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